UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/056,287	01/23/2002	Burnell G. West	M-12401 US	9790

7590 07/21/2003

Deborah Winocur
4057 Amaranta Avenue
Palo Alto, CA 94306

EXAMINER	
LE, JOHN H	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 07/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/056,287	WEST, BURNELL G.	
	Examiner	Art Unit	
	John H Le	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Objections

1. Claims 6-8 are objected to because of the following informalities:

Claim 6, line 1, after "distributing", insert –events in the primary event stream--.

Claim 7, line 1, after "distributing", insert –events in the primary event stream--.

Claim 8, line 1, after "distributing", insert –events in the primary event stream--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen et al. (USP 5,642,478).

Regarding claims 1 and 10, Chen et al. teach a circuit for time stamping events, the circuit comprising: node controller 38, which read on an event stream distributor coupled to receive the primary event stream (38 receiving 44, Fig.1); and a plurality of timestamp circuits (Col.8, lines 6-13, Col.11, lines 43-45, lines 53-55), each timestamp circuit coupled to receive a respective secondary event stream from the event stream distributor (38 distributing second event, Fig.1).

4. Claims 1-5 and 10-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Adelmann et al. (USP 4,894,823).

Regarding claims 1 and 10, Adelmann et al. teach a circuit for time stamping events, the circuit comprising: a digital line interface unit 117, which read on an event stream distributor coupled to receive signal from a receive access module 116, which read on the primary event stream (117 receiving 116, Fig.1); and a plurality of timestamp circuits (Col.2, lines 5-26, Col.6, lines 3-8), each timestamp circuit coupled to receive a respective secondary event stream 118 from the event stream distributor 117 (117 distributing second event 118, Fig.1).

Regarding claims 2 and 11, Adelmann et al. teach an event rate in each of the secondary event streams is lower than an event rate in the primary event stream (Col.5, lines 62-67).

Regarding claims 3 and 12, Adelmann et al. teach the relative timing of the events in the primary event stream is maintained in each of the secondary event streams (Col.2, lines 5-26, Col.6, lines 3-8).

Regarding claims 4 and 13, Adelmann et al. teach the primary event stream is a differential signal (116-1 through 116-X, Col.5, lines 51-61).

Regarding claims 5 and 14, Adelmann et al. teach the secondary event streams are differential signals (118-1 through 118-x, Col.5, lines 62-67).

5. Claim 26-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Fransson (USP 5,940,467).

Regarding claims 26-29, Fransson teaches a counting circuit, the circuit comprising: a first counter 31 coupled to receive the signal (Fig.1); and a first plurality of gates 71, 72, 73, 74, 75, 76, each gate of the first plurality of gates coupled to receive

the signal and each gate of the first plurality of gates coupled to receive a respective control signal from the first counter 31 (Fig.2, Fig.5A), wherein the first plurality of gates are AND gates, wherein the signal is a differential signal, wherein the signal is a single-ended signal (Col.4, lines 39-65, Col.7, lines 32-67).

Regarding claim 30, Fransson teaches the counter is a Johnson counter (Col.2, lines 5-7).

Regarding claim 31, Fransson teaches the counter is an N-bit counter (Col.2, lines 5-7, Col.4, lines 14-19, Col.5, lines 43-45).

Regarding claim 32, Fransson teaches a second counter 50-1, 50-2, 50-3, 50-4 coupled to receive the primary event stream (Fig.2); and a second plurality of gates of registers 99-1, 99-2, 99-3, 99-4, each gate of the second plurality of gates coupled to receive the signal and each gate of the second plurality of gates coupled to receive a respective control signal from the second counter (Fig.8, Col.12, lines 45-65).

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 20-25, 40-41 are rejected under 35 U.S.C. 102(e) as being anticipated by Boerker (US 2003/0035502 A1).

Regarding claim 20, Boerker teaches a data reception circuit for receiving a serial input data stream with a high data transfer rate, the method comprising: receiving the primary event stream 1; a data stream separation circuit 4 distributing rising edge events in the primary event stream among a first plurality of secondary event streams ([0057]); a asynchronously clocked register array 8 recording an arrival time of each event in the first plurality of secondary event streams with respect to a reference clock ([0058]); the data stream separation circuit 4 distributing falling edge events in the primary event stream among a second plurality of secondary event streams ([0057]); and recording an arrival time of each event in the second plurality of secondary event streams with respect to the reference clock ([0058]).

Regarding claim 21, Boerker teaches an event rate in each secondary event stream of the first plurality and the second plurality of secondary event streams is lower than an event rate in the primary event stream ([0057]).

Regarding claim 22, Boerker teaches the primary event stream is a differential signal ([0055]).

Regarding claim 23, Boerker teaches each secondary event stream of the first plurality and the second plurality of secondary event streams are differential signals ([0055]).

Regarding claim 24, Boerker teaches distributing rising edge events comprises selectively enabling a first plurality of gates and distributing falling edge events comprises selectively enabling a second plurality of gates ([0066]).

Regarding claim 25, Boerker teaches distributing rising edge events comprises selectively enabling a first plurality of gates using a first counter 8 that is clocked by the primary event stream and distributing falling edge events comprises selectively enabling a second plurality of gates using a second counter 17 that is clocked by the primary event stream ([0067]).

Regarding claims 40-41, Boerker teaches a method comprising: receiving a signal having events at N gates; selectively enabling each of the N gates such that a first event passes through a first gate, a second event passes through a second gate, a third event passes through a third gate, and so on, until an Nth event passes through a Nth gate; and recording an arrival time of each event with respect to a reference clock, wherein selectively enabling each of the N gates comprises: clocking a counter using the signal; and selectively enabling each of the N gates using a plurality of output signals generated by the counter ([0056],[0060],[0066], Fig.1, Fig.2).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 6-9, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adelmann et al. (USP 4,894,823) in view of Boerker (US 2003/0035502 A1).

Regarding claims 6 and 7, Adelmann et al. fail to teach distributing events in the primary event stream comprises selectively enabling a plurality of gates using a counter

that is clocked by the primary event stream such that a first event in the primary event stream passes through a first gate, a second event in the primary event stream passes through a second gate, and so on until an Nth event in the primary event stream passes through an Nth gate, wherein N is a positive integer.

Boerker teaches distributing events in the primary event stream comprises selectively enabling a plurality of gates using a counter that is clocked by the primary event stream such that a first event in the primary event stream passes through a first gate, a second event in the primary event stream passes through a second gate, and so on until an Nth event in the primary event stream passes through an Nth gate, wherein N is a positive integer ([0056],[0060],[0066], Fig.1, Fig.2).

Regarding claim 8, Boerker teaches distributing rising edge events in the primary event stream among a first plurality of secondary event streams; and distributing falling edge events in the primary event stream among a second plurality of secondary event streams ([0057]).

Regarding claims 9 and 19, Boerker teaches registering the events in each of the secondary event streams ([0055]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include step of distributing events in the primary event stream comprises selectively enabling a plurality of gates using a counter that is clocked by the primary event stream as taught by Boerker in a time stamping for packet system nodes of Adelmann et al. for the purpose of providing an increasing transfer rate, data or

information is transferred via a transfer channel in shorter and shorter times (Boerker, [0005]).

10. Claims 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adelmann et al. (USP 4,894,823) in view of Fransson (USP 5,940,467).

Regarding claims 15-18, Adelmann et al. fail to teach a first counter coupled to receive the primary event stream; and a first plurality of gates coupled to the first counter, wherein the first counter is a Johnson counter, wherein the first counter is an N-bit counter, a second counter coupled to receive the primary event stream; and a second plurality of gates coupled to the second counter, a plurality of registers, each register operable to register events of one or more secondary event streams.

Fransson teaches a first counter 31 coupled to receive the primary event stream; and a first plurality of gates 71, 72, 73, 74, 75, 76 coupled to the first counter (Fig.1, Fig.2, Fig.3A), wherein the first counter is a Johnson counter, wherein the first counter is an N-bit counter (Col.2, lines 5-7), second counters 50-1, 50-2, 50-3, 50-4 coupled to receive the primary event stream (Fig.2); and a second plurality of gates of registers 99-1, 99-2, 99-3, 99-4 coupled to the second counter, each register operable to register events of one or more secondary event streams (Fig.8, Col.12, lines 45-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a counter, plurality of gates coupled to the counter, wherein the counter is a Johnson counter, wherein the counter is an N-bit counter as taught by Fransson in a time stamping for packet system nodes of Adelmann et al. for

the purpose of providing a counting circuit, the resolution of which is equal to the cycle time of the first clock signal applied to the counting circuit (Fransson, Col.2, lines 46-48).

11. Claims 33-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fransson (USP 5,940,467) in view of Boerker (US 2003/0035502 A1).

Regarding claims 33-34, Fransson teaches a circuit comprising: a first counter 31 having an input coupled to receive a first output signal (Fig.1); a plurality of gates 71, 72, 73, 74, 75, 76, each gate having a input coupled to receive a respective output signal from the first counter 31 (Fig.2, Fig.5A), wherein the first plurality of gates are AND gates, wherein the signal is a differential signal (Col.4, lines 39-65, Col.7, lines 32-67).

Regarding claim 35, Fransson teaches the counter is a Johnson counter (Col.2, lines 5-7).

Regarding claim 36, Fransson teaches the counter is an N-bit counter (Col.2, lines 5-7, Col.4, lines 14-19, Col.5, lines 43-45).

Regarding claim 39, Fransson teaches a second counter 50-1 having an input 92-1 coupled to receive a second output signal from the signal generator 70; and a second plurality of AND gates, each AND gate having a input coupled to receive a respective output signal from the second counter (Col.7, lines 32-67, Fig.8, Col.12, lines 45-65).

Fransson fails to teach a buffer 4 having an input coupled to receive an input signal, the first counter having an input coupled to receive a first output signal from the

buffer; a plurality of gates, each gate having a first input coupled to receive the first output signal from the buffer.

Boerker teaches a buffer 4 having an input coupled to receive an input signal (Fig.1, [0058]); a counter 8 having an input 7 coupled to receive a first output signal 5 from the buffer 4 (Fig.1, [0058]); a plurality of gates 26-1 to 26-4, each gate having a first input 7-1 coupled to receive the first output signal 5-1 from the buffer 4 ([0060]).

Regarding claims 37-38, Boerker teaches the first output signal from the buffer 4 includes a plurality of rising edges and each rising edge is used to clock the first counter 8; a plurality of falling edges and each falling edge is used to clock the first counter 8 (Fig.1, [0057]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a buffer 4, a counter 8, plurality of gates 26-1 to 26-4 as taught by Boerker in a counting circuit of Fransson for the purpose of providing an increasing transfer rate, data or information is transferred via a transfer channel in shorter and shorter times (Boerker, [0005]).

12. Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Boerker (US 2003/0035502 A1) in view of Fransson (USP 5,940,467).

Regarding claim 42, Boerker fails to teach the gates are AND gates.

Fransson teaches the gates 171, 173 are AND gates (Col.7, lines 32-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the gates 171, 173 are AND gates as taught by Fransson in a data reception circuit of Boerker for the purpose of providing a counting circuit, the

resolution of which is equal to the cycle time of the first clock signal applied to the counting circuit (Fransson, Col.2, lines 46-48).

Other Prior Art

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Aramaki (USP 5,485,457) disclose a packet switch system capable of reducing a delay time for each packet.

Andersson et al. (USP 5,764,524) disclose a method and apparatus for detection of missing pulses from repetitive pulse train.

Contact Information

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Le whose telephone number is (703) 605-4361. The examiner can normally be reached on Monday to Friday from 9:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. John Barlow, can be reached at (703) 308-3126. The facsimile number for Technology Center 2800 is (703) 308-5841.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist of the Technology Center whose telephone number is (703) 308-0956.

John H. Le

Patent Examiner-Group 2863

June 31, 2003

John Barlow
Supervisory Patent Examiner
Technology Center 2800